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APPLICATION

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METHOD AND SYSTEM FOR DETERMINING OVERLAY TOLERANCE

Background Of The Invention

Field of the Invention

The present invention generally relates to photolithography processes, and more specifically, to a method and system for determining overlay tolerances in photolithographic processes.

Prior Art

Photolithography has a broad range of industrial applications, including the manufacture of semiconductors, flat panel displays, micromachines and disk heads. In many of these applications, multiple patterns are formed over, or on top of, one another. For example, generally speaking, integrated circuits may be made by using a series of photolithographic steps to form several layers of patterns on an underlying semiconductor substrate on which the integrated circuit is being made. Each layer may include patterns that are formed on or above patterns of one or more lower layers.

In many cases, patterns must be carefully aligned with lower patterns on the substrate. It is not necessary that these patterns be perfectly aligned, however, and some tolerance is permissible. Determining the proper tolerance between these patterns is an important aspect of the lithographic process. On the one hand, a tolerance that is too low, or tight, may significantly increase the cost and reduce the efficiency of the lithography process without any associated benefit in the performance or quality of the fabricated

semiconductor. On the other hand, tolerances that are too high, or loose, may produce degraded product.

Various techniques are known to determine the optimum sizes of the patterns that are formed on the substrate. Process window experiments in photolithography typically consist of focus exposure matrices (which have no direct bearing on yield) or wafer striping; varying image sizes across the wafer to determine the optimum image size, which produces the best yielding chips. Striping provides image size tolerance by printing too large and too small, neither of these procedures consider overlay tolerance.

Summary Of The Invention

An object of this invention is to provide a method and system for determining overlay tolerances in photolithography processes.

Another object of the present invention is to provide a tool to determine true overlay tolerance at any image size.

With particular reference to Figure 1, the present invention involves providing a product wafer, a portion of which is shown in the Figure. A planar insulating layer is deposited on the wafer. The insulating layer may be a chemical-vapor deposited (CVD) silicon oxide and is deposited to a thickness that is typically used on product wafers, such as between 3000 and 8000 Angstroms. Next, a photoresist layer is deposited on the product wafer, and this photoresist layer is then exposed to ultraviolet light through a first reticle. The first reticle is stepped across the wafer, for example by using a step-and-repeat tool, to form a series of images or patterns on the photoresist. This pattern is then transferred into the oxide using an etch process, and the features are filled with a conductive material. More insulator (oxide or low-K dielectric) is coated on the wafer,

and the lithographic step begins again using a different reticle with a corresponding pattern. This process is repeated many times and various patterns are positioned over other patterns.

The present invention studies the interaction of image size and feature misalignment. Prior to this invention, the only way to attain this information was to process a large number of lots and to create a trend of image size and alignment vs. yield. The present invention solves the problem by determining the overlay tolerance based on yield data from a single lot. The design can then be altered or the overlay limit can be tightened (or relaxed) based on failure analysis of the regions/features that are most sensitive to misalignment.

Further benefits and advantages of the invention will become apparent from a consideration of the following detailed description, given with reference to the accompanying drawings, which specify and show preferred embodiments of the invention.

Brief Description Of The Drawings

Figure 1 illustrates a portion of a wafer.

Figure 2 is a flow chart showing a preferred method of implementing this invention.

Figure 3 illustrates the results of exposing the wafer at different critical dimensions.

Detailed Description Of The Preferred Embodiments

The preferred embodiment of this invention is now described in detail for using a two-dimensional scaling plot for efficiently and accurately determining the overlay tolerance when exposing photoresist layers on a wafer using a step-and-repeat or step-and–scan

exposure tool. The overlay tolerance may then be used as input to the software or algorithm in the exposure tool during the photolithography process.

With particular reference to Figure 1, the present invention involves providing a product wafer, a portion of which is shown at 10. A planar insulating layer is deposited on the wafer. This insulating layer may be a chemical-vapor deposited (CVD) silicon oxide and is deposited to a thickness that is typically used on product wafers, such as between 3000 and 8000 Angstroms. Next, a photoresist layer is deposited on the pilot wafer, and this photoresist layer is then exposed to radiation through a first reticle. The first reticle is stepped across the pilot wafer, for example by using a step-and-repeat tool, to form a series of images or patterns on the photoresist. The above-process may be repeated a number of times to form a series of layers of patterns on the wafer. In this procedure, typically, various patterns are positioned over other patterns.

As mentioned above, the present invention determines the effect of critical dimension (CD) on overlay tolerance. The invention utilizes the principal that this tolerance is a function of image size; therefore, increasing the image size reduces the overlay tolerance and decreasing critical dimension increases the overlay tolerance. For instance, tightening the overlay tolerance by 10nm is virtually equivalent to reducing the critical dimension by 20 nm because overlay includes both a positive and a negative factor.

With reference to Figures 1-3, this invention determines the effect of critical dimension on overlay tolerance by exposing wafer 10 at different critical dimensions (above, below and at optimum image size), and varying the overlay across the wafer by intentionally increasing the magnification. The result is a different overlay/CD value for each chip involved. The wafer will exhibit a region of good chips transitioning to a region of bad chips. The good region will be larger for the smaller image size wafers. The overlay at which the bad region begins is the limit for that particular image size, thus functional yield dictates tolerance.

The procedure is straightforward when intentionally misaligning a single implant level. In the case of aligning to plural levels, if a level that is used for future level alignment is itself misaligned, then that future level is preferably misaligned the same magnitude but in the opposite direction (-1 instead of +1) in order to isolate the level in question.

The present invention thus provides process engineers with a valuable tool to determine the true overlay tolerance at any image size. If the technology requirements force a larger CD, this process will allow the engineer to find the proper tolerance rather than continue using the previous specification and risk degraded yield.

While it is apparent that the invention herein disclosed is well calculated to fulfill the objects stated above, it will be appreciated that numerous modifications and embodiments may be devised by those skilled in the art, and it is intended that the appended claims cover all such modifications and embodiments as fall within the true spirit and scope of the present invention.